

Appln No. 09/641,930

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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A video transport processor comprising:

an input for receiving one or more compressed data streams;

means for extracting MPEG video data from the compressed data streams;

means for storing the MPEG video data in an external memory; and

means for generating a table of MPEG start codes to index the MPEG video data stored in the external memory,

wherein said table of MPEG start codes is used to access the MPEG video data in the external memory during decoding of the MPEG video data.

2. (Previously Presented) A video transport processor comprising:

an input for receiving one or more compressed data streams;

means for extracting video data from the compressed data streams;

means for storing the video data in an external memory; and

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means for generating a start code table to index the video data stored in the external memory,

wherein the video data includes MPEG-2 video data comprising a plurality of SLICES, and the video transport processor further comprises means for aligning a start of said plurality of SLICES to a suitable boundary in the external memory when storing the MPEG-2 video data in the external memory.

3. (Canceled)

4. (Currently Amended) The system of [~~claim 3~~] claim 11 wherein the core transport processor, the first satellite transport processor and the second satellite transport processor are integrated on an integrated circuit chip.

5. (Canceled)

6. (Currently Amended) The system of [~~claim 3~~] claim 11 wherein the data related to the compressed data streams include clock reference data.

7. (Canceled)

8. (Currently Amended) The system of [~~claim 7~~] claim 11 wherein [~~the one or more MPEG~~] said at least one MPEG-2 Transport [~~streams include~~] stream includes at least one in-band stream and at least one out-of-band stream.

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9. (Canceled)

10. (Currently Amended) The system of ~~[claim 9]~~ claim 11 further comprising an MPEG-2 video decoder for reading the video data from the memory block and decoding the video data.

11. (Currently Amended) ~~[The system of claim 9]~~

A system comprising:

a core transport processor for receiving a plurality of compressed data streams;

a first satellite transport processor for receiving at least one of the compressed data streams and extracting video data; and

a second satellite transport processor for receiving at least one of the compressed data streams and extracting audio data,

wherein the core transport processor provides data related to the compressed data streams to at least one of the first satellite transport processor and the second satellite transport processor,

wherein the first satellite transport processor stores the video data in a memory block and generates a start code table to index the video data stored in the memory block,

wherein the plurality of compressed data streams include at least one MPEG-2 Transport stream, and

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wherein the video data includes a plurality of SLICES, and the start code table is used to index the video data, SLICE by SLICE.

12. (Original) The system of claim 11 wherein the plurality of SLICES include a plurality of rows of video data in the memory block, and the start code table is used to index the video data, row by row.

13. (Original) The system of claim 11 wherein the first satellite transport processor aligns the start of each of the plurality of SLICES to a suitable boundary in the memory block when storing the video data in the memory block.

14. (Currently Amended) The system of [~~claim 9~~] claim 11 wherein the first satellite transport processor processes down to and including a SLICE layer of said at least one MPEG-2 Transport stream.

15. (Currently Amended) The system of [~~claim 3~~] claim 11 wherein the video data includes at least one HDTV video.

16. (Canceled)

17. (Canceled)

18. (Currently Amended) The method of processing a plurality of transport streams of [~~claim 16~~] claim 23 wherein

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the step of transferring data related to the compressed data streams comprises the step of transferring clock reference data.

19. (Canceled)

20. (Currently Amended) The method of processing a plurality of transport streams of ~~[claim 19]~~ claim 23 wherein the step of receiving ~~[one or more MPEG Transport streams]~~ at least one MPEG-2 Transport stream comprises the steps of receiving at least one in-band stream and receiving at least one out-of-band stream.

21. (Canceled)

22. (Currently Amended) The method of processing a plurality of transport streams of ~~[claim 21]~~ claim 23 further comprising the steps of reading the video data from the memory block and decoding the video data.

23. (Currently Amended) ~~[The method of processing a plurality of transport streams of claim 21]~~

A method of processing a plurality of transport streams using a system with multiple transport processors comprising the steps of:

receiving a plurality of compressed data streams at a core transport processor;

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receiving at least one of the plurality of compressed data streams at a first satellite transport processor, and extracting video data;

receiving at least one of the plurality of compressed data streams at a second satellite transport processor, and extracting audio data;

transferring data related to the compressed data streams from the core transport processor to at least one of the first satellite transport processor and the second satellite transport processor;

storing the video data in a memory block; and

generating a start code table to index the video data stored in the memory block,

wherein the step of receiving the plurality of compressed data streams comprises the step of receiving at least one MPEG-2 Transport stream, and

wherein the step of reading the video data includes the step of indexing the video data, SLICE by SLICE.

24. (Currently Amended) [~~The method of processing a plurality of transport streams of claim 22~~]

A method of processing a plurality of transport streams using a system with multiple transport processors comprising the steps of:

receiving a plurality of compressed data streams at a core transport processor;

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receiving at least one of the plurality of compressed data streams at a first satellite transport processor, and extracting video data;

receiving at least one of the plurality of compressed data streams at a second satellite transport processor, and extracting audio data;

transferring data related to the compressed data streams from the core transport processor to at least one of the first satellite transport processor and the second satellite transport processor;

storing the video data in a memory block;

generating a start code table to index the video data stored in the memory block;

reading the video data from the memory block; and

decoding the video data,

wherein the step of receiving the plurality of compressed data streams comprises the step of receiving at least one MPEG-2 Transport stream, and

wherein the video data is stored in the memory block as rows, and the step of reading the video data includes the step of indexing the video data, row by row.

25. (Currently Amended) [~~The method of processing a plurality of transport streams of claim 17~~]

A method of processing a plurality of transport streams using a system with multiple transport processors comprising the steps of:

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receiving a plurality of compressed data streams at a
core transport processor;

receiving at least one of the plurality of compressed
data streams at a first satellite transport processor, and
extracting video data;

receiving at least one of the plurality of compressed
data streams at a second satellite transport processor, and
extracting audio data;

transferring data related to the compressed data
streams from the core transport processor to at least one of the
first satellite transport processor and the second satellite
transport processor;

storing the video data in a memory block; and

generating a start code table to index the video data
stored in the memory block,

wherein the step of storing the video data comprises
the step of aligning a start of each of the plurality of SLICES
to a suitable boundary in the memory block.

26. (Currently Amended) The method of processing a
plurality of transport streams of [~~claim 16~~] claim 23 wherein
the step of extracting video data comprises the step of
extracting at least one HDTV video.

27. (Currently Amended) A system comprising:

a core transport processor for receiving a plurality
of compressed data streams;

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a satellite transport processor for receiving at least one of the compressed data streams and for extracting video data, the video data including a plurality of SLICES;

an MPEG-2 video decoder for decoding the video data to generate decoded video data; and

a video compositor for blending the decoded video data with graphics,

wherein the satellite transport processor generates a start code table to index the video data and aligns the plurality of SLICES to a suitable boundary in an external memory.

 28. (Original) The system of claim 27 wherein the core transport processor, the satellite transport processor, the MPEG-2 video decoder and the video compositor are integrated on an integrated circuit chip.

29. (Original) The system of claim 27 wherein the video data include SDTV video data.

30. (Original) The system of claim 27 wherein the video data include HDTV video data.

31. (New) A video transport processor comprising:
an input for receiving an MPEG Transport stream including MPEG video data comprising a plurality of SLICES;
a transport processor for processing headers in the MPEG Transport stream; and


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a start code alignment module for storing the MPEG video data in an external memory, for aligning a start of the plurality of SLICES to a suitable boundary in the external memory when storing the MPEG video data in the external memory, and for generating a start code table to index the MPEG video data stored in the external memory.

32. (New) The video transport processor of claim 31, further comprising a switch for providing the MPEG Transport stream to the transport processor or the start code alignment module.

 33. (New) The video transport processor of claim 32, wherein the switch provides the MPEG Transport stream first to the transport processor, and provides the MPEG Transport stream to the start code alignment module after one or more headers have been processed.

34. (New) The video transport processor of claim 31, further comprising a memory control interface for interfacing between the start code alignment module and the external memory.

35. (New) The video transport processor of claim 31, wherein the memory control interface includes a buffer for storing at least a portion of the MPEG video data prior to providing it to the external memory.

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36. (New) The video transport processor of claim 31,
wherein one or more zeros are added to at least one of the
SLICES to align another one of the SLICES to the suitable
boundary in the external memory.
